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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **06 / 08 / 2024** | **Batch No:** | **C3** |
| **Faculty Name:** | **Bharathi Narayan** | **Roll No:** | **16010123217** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 4**

**Title: 4-bit magnitude comparator**

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| **Aim and Objective of the Experiment:** |
| To design and implement 1-bit comparator using logic gates and verify 4-bit magnitudecomparator using IC 7485 |

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| **COs to be achieved:** |
| **CO2**: Use different minimization techniques and solve combinational circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Comparator:** The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.    **1-bit Comparator Implementation Details:**  **Truth Table**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **A** | **B** | **A<B** | **A=B** | **A>B** | | **0** | **0** | **0** | **1** | **0** | | **0** | **1** | **1** | **0** | **0** | | **1** | **0** | **0** | **0** | **1** | | **1** | **1** | **0** | **1** | **0** |   **From the Truth Table:**  **(A<B) = (A<B) is true when A=0, B=1.**  **(A=B) = (A=B) is true when A=B i.e both are either 0 or 1**  **(A>B) = (A>B)** **is true when A=1, B=0**  **Logic Diagram of 1-bit Comparator**  Logic circuit design of a digital 1-bit comparator ...  **Four Bit Magnitude Comparator Implementation Details**  **Pin Diagram of IC 7485**  7485 Datasheet  **Logic Diagram of IC 7485**    **Comparing Table**  A table with numbers and letters  Description automatically generated |

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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 7485 on the trainer kit. 2. Connect 1st input no. to A3-A0 input slot and 2nd to B3-B0. 3. Connect the output YA>B , YA<B and YA=B to the output indicators. 4. Switch ON the power supply and monitor the output for various input combinations. |
| **Post Lab Subjective/Objective type Question** |
| 1. Design 2-bit magnitude comparator.   Ans. Truth Table          Logic Diagram:-     1. How can we implement 5-bit magnitude comparator using IC 7485.   Ans. As we know IC 7485 is a 4-bit comparator that means we have four input lines. As to  Make it a 5-bit comparator we need five input lines which can be achieved by cascading the  A<B and A>B lines    The use of XOR gate is to get the output of A=B as when both A>B and A<B are zero the  Output of XOR gate is 1.   1. Virtual Lab for 8 bit digital comparator using Virtual Lab ([Digital Logic Design)](https://de-iitr.vlabs.ac.in/) Perform simulation.   [Virtual Labs (vlabs.ac.in)](https://dld-iitb.vlabs.ac.in/exp/eight-bit-digital-comparator/simulation.html)  Give feedback for the experiments of virtual lab using somaiya email id.  A=B    A>B    A<B |

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| **Conclusion:** |
| In this experiment we understood how IC’s can be used to compare 1-bit, 2-bit and 4-bit numbers  also 5-bit and 8-bit numbers by doing post lab questions |

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| **Signature of faculty in-charge with Date:** |